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Procedia Engineering 23 (2011) 417 – 422

Procedia Engineering

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PEEA 2011 Shenzhen

Design and Simulation on a Novel UPQC Topology & its Control Strategy

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Abstract

A novel single-phase Unified Power Quality Controller (UPQC) topology is proposed in this paper, which can effectively solve some kinds of power quality problems from the load or from the power side. The new topological structure of single-phase UPQC and its working principle are introduced firstly. Then, the control methods especially for the load voltage compensation and grid harmonic current compensation are discussed. Finally, simulation models are built up with SimPower Systems Blockset of MATLAB/SIMULINK and results verify the effectiveness of this new topology and control strategy.

Selection and/or peer-review under responsibility of PEEA

Keywords: single-phase UPQC; control method; simulation

1. Introduction

A UPQC can be used not only to compensate harmonic voltage, reactive power, negative-sequence current caused by nonlinear load, but also to relieve customers from those bad effects resulting from the unbalance and amplitude fluctuation of grid voltage. Accordingly UPQC has been studied widely[1-4]. However, a conventional UPQC uses a unified series-shunt structure and inevitably consists of a series transformer that leads to such problems as big volume, heavy weight, high cost and complex control. A solution is to use a UPS without transformer and containing a PFC stage, which can realize similar functions. Unfortunately, this kind of structures is confronted with decreasing efficiency owing to the two-stage power converting[5, 6]. Considering the above limitations, this paper puts forward a novel single-phase UPQC topology, which combines the characteristics of both UPS and conventional UPQC. In this

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doi:10.1016/j.proeng.2011.11.2523

new topology, a high-speed bidirectional switch is applied to replace the series transformer in a conventional UPQC, three switches near to the load side work coordinately to overcome the undesirable effects brought by voltage sags and swells, a bridge converter is used near to the power side to realize the compensation of both active power and harmonic current. This novel UPQC is characteristic of simple structure, small volume, low cost and has promising applications in customer power apparatus, UPS and so on.

In this paper, a basic introduction about the novel single-phase UPQC topology is presented first. Then detail information is demonstrated about the performing principles esp. the two key control algorithms, that is, the volt-second balance control algorithm used to realize the stabilization of the load voltage, and the compensation control algorithm applied to compensate harmonic current on the power side. Finally, a simulation model of this novel UPQC is set up in MATLAB/SIMULINK to verify its viability.

2. Topology and basic principle of the novel single-phase UPQC

The main topology of this novel UPQC is shown in Fig. 1. It is composed of two core parts, the half-bridge input conversion stage in the left dashed box and the half-bridge output voltage conversion stage in the right dashed box. As shown in this figure, the input conversion stage consists of switches S_1, S_2, and an input LC filter circuit which is connected to the grid. This part is mainly used to compensate harmonic current and provide part of load active power. As to the output voltage conversion circuit, it is composed of two half-bridge switches S_3, S_4, a bidirectional switch S_5 and an output LC filter circuit which is connected to the load. This part realizes the function of stabilizing the output voltage and improving the power quality on the load side by effectively dealing with the grid voltage sags and swells. Furthermore, these two parts are connected together by two DC-bus capacitors C_3 and C_4, each stabilizing its own voltage to U_d.

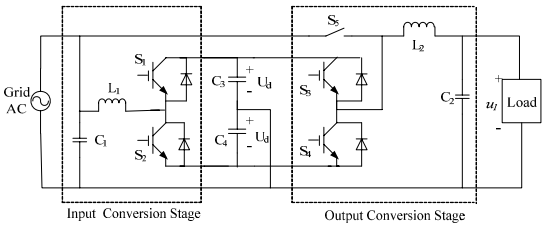

Fig. 1. The topology of a novel single-phase UPQC

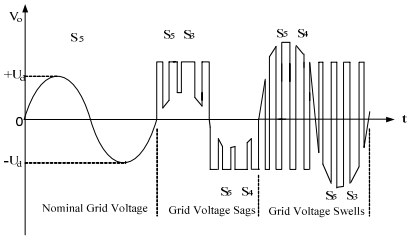

Fig. 2. Output voltage regulation mode before output filter

3. Work principle and control algorithm of the output voltage conversion stage

In order to provide a stable output voltage and decrease switching losses, this design of output conversion stage utilizes the structure of an off-line UPS and that of a Dynamic Voltage Regulator (DVR). The work principles of the output voltage conversion are introduced in detail as follows and illustrated in Fig. 2, too.

Operation mode 1: When the grid voltage is within the range of 90% and 110% of the rated voltage value, the output voltage conversion stage makes full use of the grid power. This means that S_5 is on, and S_3, S_4 are both off without drive signals. This is shown as normal grid voltage in Fig. 2 and load power is supplied directly by the grid in this situation.

Operation mode 2: When the grid voltage is below 90% of the rated voltage, S_3, S_4, S_5 work in a concerted way so that the output voltage waveform approaches the rated sine wave. In the positive half

cycle of the grid voltage, S_4 is off, and S_3, S_5 are on complementarily. While in the negative half cycle of the grid voltage, S_3 is off, and S_4, S_5 are on complementarily. This is shown as grid voltage sags in Fig. 2 and the waveform will be close to sine after passing L_2C_2 filter.

Operation mode 3: When the grid voltage is above 110% of the rated voltage, S_3, S_4, S_5 work in a similar way. In the positive half cycle of the grid voltage, S_3 is off, and S_4, S_5 work complementarily. While in the negative half cycle of the grid voltage, S_4 is off, and S_3, S_5 work complementarily. This is shown as grid voltage swells in Fig. 2 and the waveform will be close to sine after passing L_2C_2 filter.

Obviously, operation modes 2 and 3 correspond to the processes of overcoming the undesirable effects of grid voltage sags and swells respectively. Fig. 2 demonstrates the output voltage waveform and corresponding information about the conducting switches in each operation mode.

In the operation modes 2 and 3, the constant-frequency PWM is adopted and the L_2C_2 filter circuit is simple to design, so, it is a key control technique to figure out the reasonable conduction time of each switch in time. In this design, volt-second balance principle is adopted to simplify the computation of the drive pulse widths. Assuming the grid voltage $u_2(t)=U_m sin(\omega t+\theta)$, the output voltage $u_1(t)=U_o sin(\omega t+\alpha)$, the DC bus voltage is $2U_d$, the duty cycle of the bidirectional switch S_5 is D, the duty cycle of S_3 and S_4 is 1-D, and the PWM period is T, the following Equation (1) can be gotten according to the voltage-second balance.

$$U_0 \sin(\omega t+\alpha)T = U_m \sin(\omega t+\theta)DT \pm U_d(1-D)T \quad (1)$$

As to the right hand of the equation above, the plus sign before the second term is valid in the positive half cycle of the grid voltage, the minus sign is valid in the negative half cycle.

From the Equation (1), D can be further derived

$$D = \frac{U_o \sin(\omega t+\alpha) - U_d}{U_m \sin(\omega t+\theta) \pm U_d} \quad (2)$$

Accordingly, this UPQC uses a DSP to sample the above voltage signals and then calculate D. And consequently DSP produces a PWM signal to drive the switch S_5 as well as the drive signals of S_3, S_4. The basic process illustrated above is shown in Fig. 3.

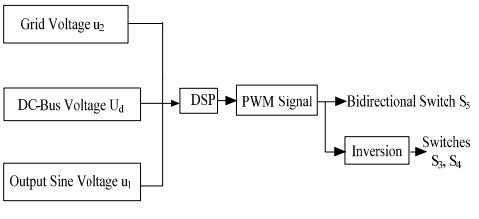

Fig. 3. Duty cycle D computation and PWM drive signals

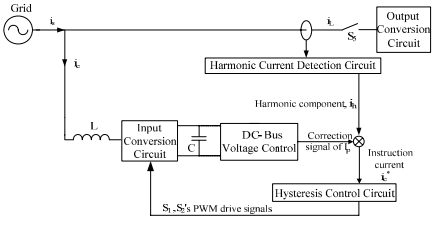

Fig. 4. Control block diagram of the input conversion circuit

4. Work principle and control algorithm of the input conversion stage

As explained above, the input conversion stage of this UPQC topology mainly aims at compensating the harmonic current produced by the output conversion stage and providing part of active power of the load to realize the stability of the DC bus voltage. Its control structure is shown as Fig. 4.

From Fig. 4, the harmonic current detection block is used to measure the current of S_5 branch, i_L, from which its active power component, reactive power component and harmonic component can be computed by several methods[7, 8]. Here, the harmonic detection method using fundamental orthogonal components is adopted to derive the harmonic component. This method is characteristic of simple, fast computation, convenient realization, and overcomes the shortcomings of the Instantaneous Reactive Power method,

which concerns more multipliers, more complex computation. Its detailed principle is illustrated as follows.

$$i_L(t) = i_p(t) + i_q(t) + i_h(t) = I_p \sin \omega t + I_q \cos \omega t + \sum_{k=3}^{\infty} I_k \cos(k\omega t + \phi_k) \quad (3)$$

In the equation above, $i_L(t)$ is denoted as the load current; $i_p(t)$ is denoted as the fundamental active power component of $i_L(t)$; $i_q(t)$ is denoted as the fundamental reactive power component of $i_L(t)$; $i_h(t)$ is denoted as the harmonic component of $i_L(t)$.

Then, after multiplying $i_L(t)$ with the sine and cosine components of the gird voltage U_s respectively (Here, assume the nominal voltage value of U_s to be 1), the following are derived:

$$i_L(t)\sin \omega t = \frac{I_p}{2}(1+\cos 2\omega t) + \frac{I_q}{2}\sin 2\omega t + \sum_{k=3}^{\infty} \frac{I_k}{2}\{\cos[(k+1)\omega t + \varphi_k] + \cos[(k-1)\omega t + \varphi_k]\} \quad (4)$$

$$i_L(t)\cos \omega t = \frac{I_q}{2}(1-\cos 2\omega t) + \frac{I_p}{2}\sin 2\omega t + \sum_{k=3}^{\infty} \frac{I_k}{2}\{\sin[(k+1)\omega t + \varphi_k] + \sin[(k-1)\omega t + \varphi_k]\} \quad (5)$$

From the Equation 4, the fundamental active power current I_p can be gotten through a low-pass filter firstly, and then the instantaneous fundamental active power current $i_p(t)$. Similarly, the fundamental reactive power current I_q and further the instantaneous reactive power current $i_q(t)$ can be derived. Finally, the instantaneous harmonic current $i_h(t)$ can be gotten by subtracting the fundamental instantaneous components from i_L according to Equation 3.

Besides the above function, it is necessary to provide some active power to the load in order to keep bus voltage U_d stable. This design applies the difference of U_d and the reference bus voltage value to perform the Proportion-Integration computation. The result is regarded as the correction signal of the active power current component I_p. Through adding I_p's correction signal $i_{p\text{-}c}$ to the harmonic component i_h, the instruction current i_c^* of the input stage is gotten. Accordingly, this instruction current i_c^* and the real compensating current i_c produced by the input conversion are applied as inputs of a hysteresis comparison control. Then, the drive signals of switches S_1, S_2 are derived. Therefore, through the whole process illustrated above, the input conversion circuit can realize to both compensate the harmonic current on the S_5 branch and provide the active power to the load from the grid[7-9]. The detailed process about the harmonic current detection and the compensation of the load current's active power component is shown in Fig. 5.

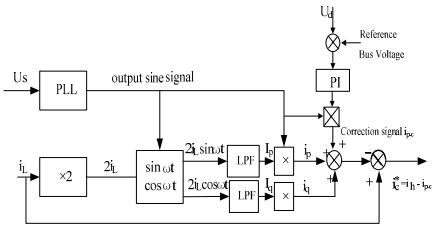

Fig.5 Harmonic current detection & compensation of i_p

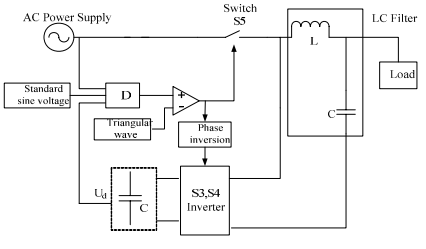

Fig. 6. MATLAB model of the output conversion stage

5. MATLAB model and simulation analysis

This paper applies the power analysis tools of MATLAB/SIMULINK to build up simulation models for this novel UPQC topology and to test the control algorithms proposed above.

The model and simulation results of the output voltage conversion stage are introduced below firstly. The MATLAB model of the output voltage conversion stage is shown in Fig. 6. In this model, the single-

phase AC rated voltage is 220V, the DC bus voltage is 260V, the switching frequency is 20 kHz, the filtering inductance is 1mH, the filtering capacitor is 2μF. This paper simulates the operation modes of grid voltage sags and swells respectively. Furthermore the ability to provide stable voltage to different loads is compared through the simulation. Fig. 7a—7c show the simulation waveforms of voltages related with the output conversion under the circumstance of the grid voltage sags. Fig. 8a—8c show the corresponding voltage waveforms under the circumstance of the grid voltage swells. From the simulation results above, it can be seen that this output conversion topology can improve the load voltage quality by the coordinate work of bidirectional switch S_5 and two half-bridge switches S_3, S_4.

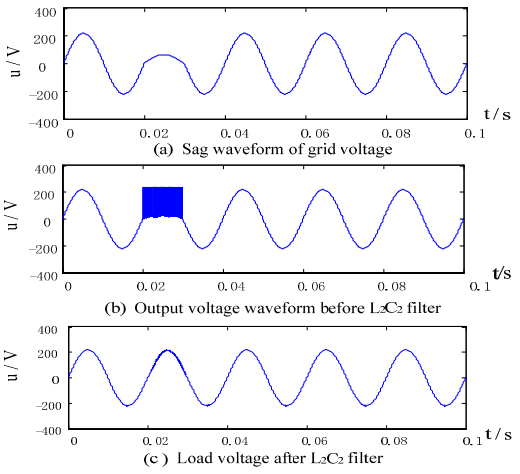

Fig.7 Simulated waveforms during sags

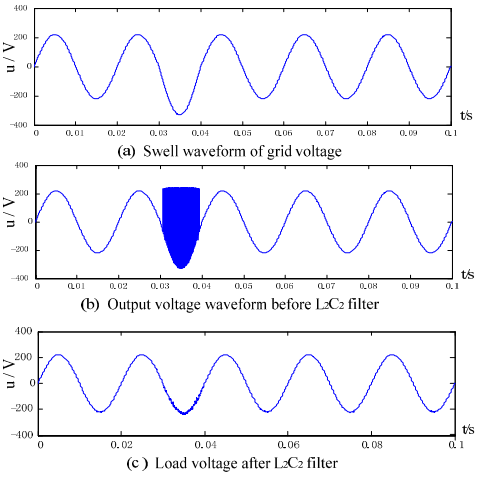

Fig.8 Simulated waveforms during swells

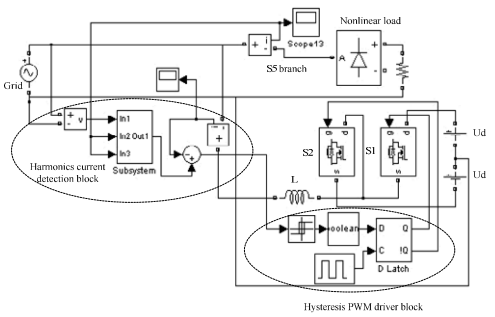

Fig. 9. Simulation model for input conversion stage

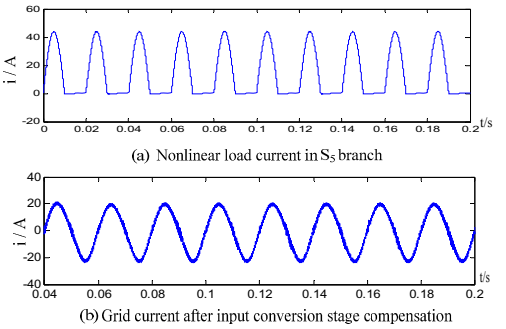

Fig. 10. Simulated waveforms of harmonic current compensation

Similarly, the model and simulation results of the input conversion stage are introduced below, too. Its MATLAB model is shown in Fig. 9. Here, this paper pays attention to verifying the function of compensating harmonic current. In our model, we set the grid voltage to 220V, the filtering inductance L_1 to 1mH, the filtering capacitor to 4μF, and assume the S_5 branch current waveform is the result of half-wave rectification. Fig. 10(a) shows the S_5 branch current waveform without the input conversion. And

Fig. 10(b) shows the S_5 branch current waveform with the input conversion. We can see that the grid current is compensated effectively.

6. Conclusion

A novel single-phase UPQC topology and its control algorithms are proposed and its effect is verified by MATLAB simulation. In this topology, a high-speed bidirectional switch replaces the series transformer so that the structure is simplified, the cost is lowered. As to the output conversion, the volt-second balance principle is used to compute the duty cycle so as to stabilize the output voltage. As to the input conversion, a fast control method can compensate harmonic current of the load and provide active power for the DC bus. Finally, the corresponding models are built up and simulated in MATLAB/SIMULINK. Simulation result shows this novel UPQC topology can prevent the undesirable effects of grid voltage sags and swells on the load effectively and realize a low-harmonic current supply.

Acknowledgements

This project is supported by the National Natural Science Foundation of China under Grant No. 50877015 and the Doctor Subject Foundation of the Ministry of Education of China under Grant No. 200802131017.

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